Solar Cell Design for Manufacturing

Ralf Jonczyk, Victor Lou[1], Shyh-Chin Huang[1], Mark D'Evelyn[1], Alysha Grenko, James Rand
GE Energy, 231 Lake Drive, Newark, DE, Ralf.Jonczyk@nrel.gov
[1]GE Global Research, Niskayuna, NY

ABSTRACT

GE Energy is commercializing a process for directionally solidifying individual molded wafers. The process has demonstrated good material utilization and very low cost, both in terms of capital equipment expense and direct material consumption. A new molded wafer furnace will be put into operation in the first quarter of 2007. Modules based on molded wafer solar cells will be marketed in the second half of 2007.

1. Objectives

The broad objectives of this DOE Photovoltaic Manufacturing R&D Program are to implement critical improvements to the process of casting individual wafers. Those improvements will lead to a novel all back interconnected module technology. The product is being developed following GE's Design for Six Sigma approach to deliver a product ready for large-scale manufacturing. Coupled with improvements in wafer quality, this program will result in modules with costs 30% lower than the industry standard cast multicrystalline wafer based products.

2. Technical Approach

The approach chosen by GE Energy is to develop a metal wrap through (MWT) solar cell made possible by the molded wafer process. Figure 1 shows the general concept of the interconnect scheme. Based on very good experience with laser cutting we have changed our initial approach from molding the holes during wafer growth to laser cutting holes. This approach can also be combined with additional efficiency enhancing process steps. The MWT project will result in a high-density module package, filling up to 95% of the module area with solar cells. The program will result in a >13% module, based on 14% efficient solar cells.

A significant reduction in silicon consumption has been achieved by making thinner wafers. Preliminary trials have demonstrated wafer thickness as low as 400μm. This cut in material consumption is in addition to the 40% reduction achieved by replacing the continuous sheet with the molded wafer process. By the end of the program, these changes will result in silicon consumption 25% better than the industry standard cast material.

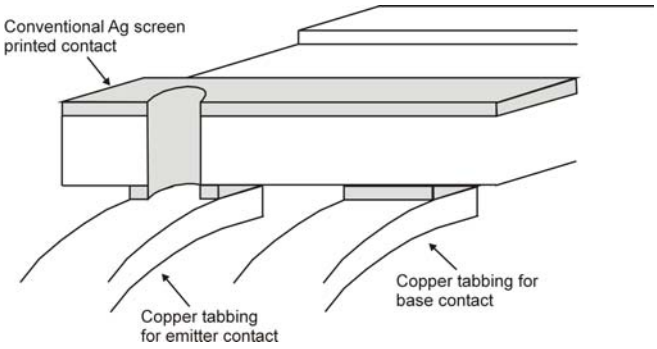

Figure 1. MWT contact scheme

3. Results and Accomplishments:

During the first phase of the program we have achieved a number of milestones towards our goals. These achievements can be separated into four main areas.

1. Thickness reduction
2. Wafer quality improvement
3. Solar cell process improvement
4. Metal wrap through process development

3.1 Thickness reduction:

As mentioned above we have achieved wafer thickness of 400μm in some trials and have stabilized our wafer thickness at about 600μm. Figure 2 shows the progress in reduction of wafer thickness and wafer thickness variation.

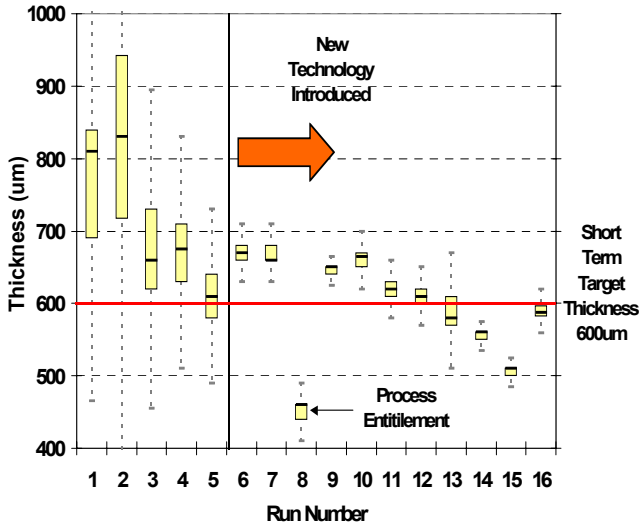

Figure 2: Process control chart showing transition to a new feedstock loading process with significant reduction in wafer weight and wafer weight variation.

3.2. Wafer quality improvement:

Molded wafer lifetimes have been historically low, ranging from 0.5μs to 2μs. In order to achieve the desired efficiency of 14%, the minority carrier lifetime should be in the range of 5μs to 10μs. We have demonstrated lifetimes in that range by both modifying our wafer growth environment and improving our getter process. Figure 3 shows a μ-PCD scan of a wafer made using an improved but not yet optimized wafer growing process. While there remains a good deal of non-uniformity the wafer shows an average lifetime improvement of more 100% over wafers produced using our current process. We have determined that a new molded wafer furnace and a new getter process are required and have purchased and installed new manufacturing equipment.

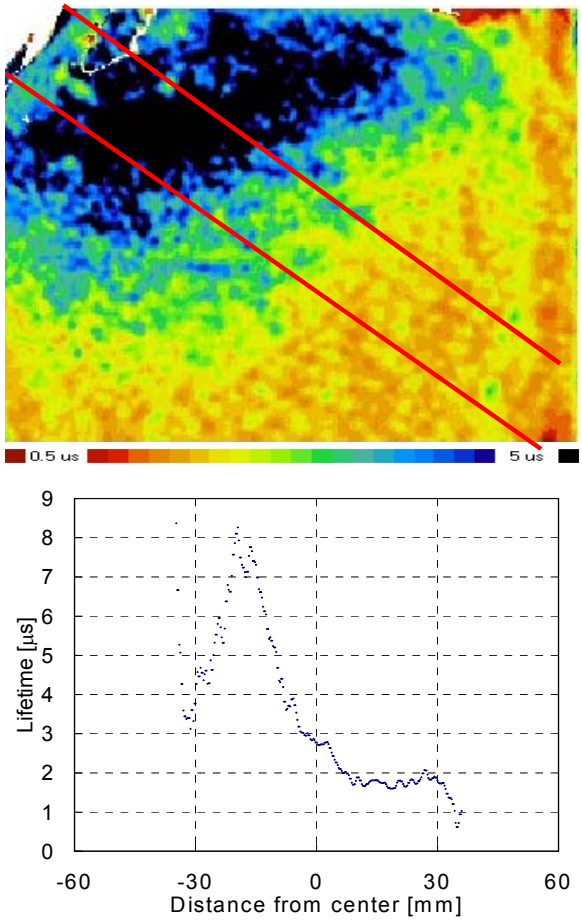

Figure 3: Left: Lifetime scan of wafer produced in laboratory furnace; Right: line-scan of lifetime between red lines. The sample size is about 5cm x 5cm.

3.3 Solar cell process improvements:

While we have been able to show high minority carrier lifetime using small wafers and experimental processes only, we have been able to increase solar cell performance by two absolute percent from 10% to 12% using large area low lifetime wafers and a state of the art solar cell manufacturing processes. Figure 4 shows a lifetime scan for a > 12 percent efficient solar cell (currently being tested by NREL for confirmation). The average minority carrier lifetime of this wafer after processing was less than 2μs (see Figure 4). We expect to achieve 14% efficiency combining state of the art solar cell processing and high lifetime molded wafers.

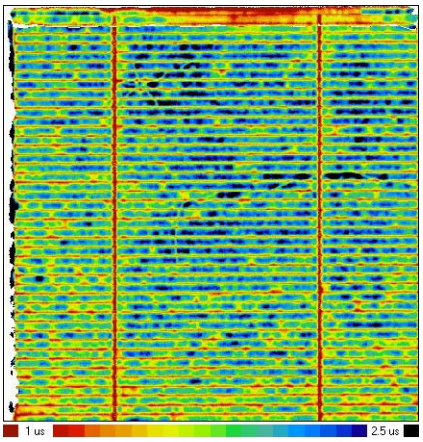

Figure 4: Left: Lifetime scan of a >12% molded wafer solar cell produced using state of the art processing

3.4 Metal wrap through process development:

To improve overall module efficiency and performance we are currently developing a metal wrap through technology. We have assembled first prototype units and are now in the process of optimizing the solar cell process and module assembly process. A significant amount of highly accelerated lifetime testing has been performed on modules and subassemblies.

4. Conclusions

The first phase of this program has brought us significantly closer to our goal of achieving low cost crystalline PV modules. Based on findings enabled by new characterization tools and our cooperation with GE's Global Research Center we have changed our initial approach of improving and upgrading our current wafer furnace to designing and purchasing a new wafer furnace which will be capable of better atmosphere and temperature control. We have demonstrated solar cell efficiency of over 12% on large wafers using standard state of the art manufacturing equipment and wafers made in our current furnace with minority carrier lifetime well below 100μm. Better minority carrier lifetime is expected in wafers made in our new machine using an improved growth environment and better thermal control. We have also assembled first back contact modules.

ACKNOWLEDGEMENTS

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